

II. Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A method of forming a dual damascene opening, comprising the steps of:

providing a structure having an overlying exposed conductive layer formed thereover;

forming a dielectric layer over the exposed conductive layer;

forming an anti-reflective coating layer over the dielectric layer;

etching the anti-reflective layer and the dielectric layer using a via opening process to form an initial via exposing a portion of the conductive layer;

forming a protective film portion over at least the exposed portion of the conductive layer; layer, the protective film portion being comprised of the elements C and H; and

patterning the anti-reflective coating layer and the dielectric layer to reduce the initial via to a reduced via and to form a trench opening substantially centered over the reduced via; the trench opening and the reduced via comprising the dual damascene opening.

2. (Currently amended) The method of claim 1, wherein the structure includes a silicon substrate or a germanium substrate; the conductive layer is comprised of copper, aluminum, gold or silver; the dielectric layer is comprised of the elements Si, O, C and/or H such as SiOCH; the anti-reflective coating layer is comprised of SiON or SiOC; ~~and the protective film portion is comprised of the elements C, H and O such as C_xH_y.~~

3. (Original) The method of claim 1, wherein the structure includes a silicon substrate; the conductive layer is comprised of copper; the dielectric layer is comprised of the elements Si, O, C and/or H; the anti-reflective coating layer is comprised of SiON;

and the protective film portion is comprised of C_2H_4 or C_2H_6 .

4. (Original) The method of claim 1, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of less than about 3.0.

5. (Original) The method of claim 1, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.0 to less than about 3.0.

6. (Original) The method of claim 1, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.5 to 2.8.

7. (Original) The method of claim 1, wherein the conductive layer has a thickness of from about 3000 to 15,000Å; the dielectric layer has a thickness of from about 2000 to 20,000Å; the anti-reflective coating layer has a thickness of from about 50 to 2000Å; and the protective film portion has a thickness of from about 50 to 2000Å.

8. (Original) The method of claim 1, wherein the conductive layer has a thickness of from about 3000 to 8000Å; the dielectric layer has a thickness of from about 2000 to 15,000Å; the anti-reflective coating layer has a thickness of from about 100 to 1500Å; and the protective film portion has a thickness of from about 200 to 1500Å.

9. (Original) The method of claim 1, wherein the via opening process is a dry etch process employing an F-based plasma.

10. (Original) The method of claim 1, wherein the via opening process is conducted under the following conditions:

temperature: from about 0 to 200°C;

pressure: preferably from about 5 to 300 mTorr;

time: preferably from about 10 to 500 seconds; and
plasma power: preferably from about 0 to 3000 W.

11. (Original) The method of claim 1, wherein the via opening process is conducted under the following conditions:

temperature: from about 0 to 100°C;
pressure: preferably from about 5 to 250 mTorr;
time: preferably from about 20 to 300 seconds; and
plasma power: preferably from about 50 to 2500 W.

12. (Original) The method of claim 1, including the step of forming an etch stop/liner layer over the exposed conductive layer.

13. (Original) The method of claim 1, including the step of forming an etch stop/liner layer over the exposed conductive layer; the etch stop/liner layer having a thickness of from about 50 to 2000Å and being comprised of the elements Si, O, N and/or C such as Si₃N₄, SiOCN, SiOC or SiC.

14. (Original) The method of claim 1, including the step of forming an etch stop/liner layer over the exposed conductive layer; the etch stop/liner layer having a thickness of from about 100 to 1000Å and being comprised of the elements Si, O, N and/or C such as Si₃N₄, SiOCN, SiOC or SiC.

15. (Currently amended) ~~The method of claim 1, wherein~~ A method of forming a dual damascene opening, comprising the steps of:

providing a structure having an overlying exposed conductive layer formed thereover;

forming a dielectric layer over the exposed conductive layer;

forming an anti-reflective coating layer over the dielectric layer;

etching the anti-reflective layer and the dielectric layer using a via opening
process to form an initial via exposing a portion of the conductive layer;
forming a protective film portion over the exposed portion of the conductive layer
~~the protective film portion is also formed~~ and over the etched anti-reflective coating
~~layer.~~ layer; and
patterning the anti-reflective coating layer and the dielectric layer to reduce the
initial via to a reduced via and to form a trench opening substantially centered over the
reduced via; the trench opening and the reduced via comprising the dual damascene
opening.

16. (Original) The method of claim 1, wherein a via plug is formed within the initial via before formation of the trench opening.

17. (Original) The method of claim 1, wherein a via plug is formed within the initial via before formation of the trench opening; the via plug being comprised of the elements C, H and/or O.

18. (Original) The method of claim 1, wherein the formation of trench opening utilizes a patterned masking layer as a mask.

19. (Original) The method of claim 1, wherein the formation of trench opening utilizes a patterned photoresist masking layer as a mask.

20. (Currently amended) ~~The method of claim 1, wherein~~ A method of forming
a dual damascene opening, comprising the steps of:

providing a structure having an overlying exposed conductive layer formed
thereover;

forming a dielectric layer over the exposed conductive layer;
forming an anti-reflective coating layer over the dielectric layer;
etching the anti-reflective layer and the dielectric layer using a via opening
process to form an initial via exposing a portion of the conductive layer;
forming a protective film portion over at least the exposed portion of the
conductive layer, the protective film portion [[is]]being comprised of an organic CVD
film; and
patterning the anti-reflective coating layer and the dielectric layer to reduce the
initial via to a reduced via and to form a trench opening substantially centered over the
reduced via; the trench opening and the reduced via comprising the dual damascene
opening.

21. (Currently amended) The method of claim [[1]]20, wherein the initial via has a width of from about 200 to 3500Å and the trench opening has a width of from about 5000Å to 100µm.

22. (Currently amended) The method of claim [[1]]20, wherein the initial via has a width of from about 800 to 2500Å and the trench opening has a width of from about 5000Å to 100µm.

23. (Original) A method of forming a dual damascene opening, comprising the steps of:

providing a silicon structure having an overlying exposed conductive layer formed thereover; the conductive layer being comprised of copper, aluminum, gold or silver;

forming a dielectric layer over the exposed conductive layer; the dielectric layer being comprised of the elements Si, O, C and/or H such as SiOCH;

forming an anti-reflective coating layer over the dielectric layer; the anti-reflective

coating layer being comprised of SiON or SiOC;

etching the anti-reflective layer and the dielectric layer using a via opening process to form an initial via exposing a portion of the conductive layer;

forming a protective film portion over at least the exposed portion of the conductive layer; the protective film portion being comprised of the elements C, H and O such as C₂H₄ or C₂H₆;

patterning the anti-reflective coating layer and the dielectric layer to reduce the initial via to a reduced via and to form a trench opening substantially centered over the reduced via; the trench opening and the reduced via comprising the dual damascene opening.

24. (Original) The method of claim 23, wherein the conductive layer is comprised of copper; and the anti-reflective coating layer is comprised of SiON.

25. (Original) The method of claim 23, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of less than about 3.0.

26. (Original) The method of claim 23, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.0 to less than about 3.0.

27. (Original) The method of claim 23, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.5 to 2.8.

28. (Original) The method of claim 23, wherein the conductive layer has a thickness of from about 3000 to 15,000Å; the dielectric layer has a thickness of from about 2000 to 20,000Å; the anti-reflective coating layer has a thickness of from about 50 to 2000Å; and the protective film portion has a thickness of from about 50 to 2000Å.

29. (Original) The method of claim 23, wherein the conductive layer has a

thickness of from about 3000 to 8000Å; the dielectric layer has a thickness of from about 2000 to 15,000Å; the anti-reflective coating layer has a thickness of from about 100 to 1500Å; and the protective film portion has a thickness of from about 200 to 1500Å.

30. (Original) The method of claim 23, wherein the via opening process is a dry etch process employing an F-based plasma.

31. (Original) The method of claim 23, wherein the via opening process is conducted under the following conditions:

temperature: from about 0 to 200°C;

pressure: preferably from about 5 to 300 mTorr;

time: preferably from about 10 to 500 seconds; and

plasma power: preferably from about 0 to 3000 W.

32. (Original) The method of claim 23, wherein the via opening process is conducted under the following conditions:

temperature: from about 0 to 100°C;

pressure: preferably from about 5 to 250 mTorr;

time: preferably from about 20 to 300 seconds; and

plasma power: preferably from about 50 to 2500 W.

33. (Original) The method of claim 23, including the step of forming an etch stop/liner layer over the exposed conductive layer.

34. The method of claim 23, including the step of forming an etch stop/liner layer over the exposed conductive layer; the etch stop/liner layer having a thickness of from about 50 to 2000Å and being comprised of the elements Si, O, N and/or C such as Si₃N₄, SiOCN, SiOC or SiC.

35. (Original) The method of claim 23, including the step of forming an etch stop/liner layer over the exposed conductive layer; the etch stop/liner layer having a thickness of from about 100 to 1000Å, and being comprised of the elements Si, O, N and/or C such as Si₃N₄, SiOCN, SiOC or SiC.

36. (Original) The method of claim 23, wherein the protective film portion is also formed over the etched anti-reflective coating layer.

37. (Original) The method of claim 23, wherein a via plug is formed within the initial via before formation of the trench opening.

38. (Original) The method of claim 23, wherein a via plug is formed within the initial via before formation of the trench opening; the via plug being comprised of the elements C, H and/or O.

39. (Original) The method of claim 23, wherein the formation of trench opening utilizes a patterned masking layer as a mask.

40. (Original) The method of claim 23, wherein the formation of trench opening utilizes a patterned photoresist masking layer as a mask.

41. (Original) The method of claim 23, wherein the initial via has a width of from about 200 to 3500Å and the trench opening has a width of from about 5000Å to 100µm.

42. (Original) The method of claim 23, wherein the initial via has a width of from about 800 to 2500Å and the trench opening has a width of from about 5000Å to 100µm.

43. (Original) A method of forming a dual damascene opening, comprising the

steps of:

providing a structure having an overlying exposed conductive layer formed thereover;

forming an etch stop/liner layer over the exposed conductive layer;

forming a dielectric layer over the etch stop/liner layer;

forming an anti-reflective coating layer over the dielectric layer;

etching the anti-reflective layer and the dielectric layer using a via opening process to form an initial via exposing a portion of the etch stop/liner layer;

removing the exposed portion of the etch stop/liner layer using a liner removal process to expose a portion of the underlying conductive layer;

forming a protective film portion over at least the exposed portion of the conductive layer;

patterning the anti-reflective coating layer and the dielectric layer to reduce the initial via to a reduced via and to form a trench opening substantially centered over the reduced via; the trench opening and the reduced via comprising the dual damascene opening.

44. (Original) The method of claim 43, wherein the structure includes a silicon substrate or a germanium substrate; the conductive layer is comprised of copper, aluminum, gold or silver; the dielectric layer is comprised of the elements Si, O, C and/or H such as SiOCH; the anti-reflective coating layer is comprised of SiON or SiOC; the etch stop/liner layer is comprised of the elements Si, O, N and/or C such as Si₃N₄, SiOCN, SiOC or SiC; and the protective film portion is comprised of the elements C, H and O.

45. (Original) The method of claim 43, wherein the structure includes a silicon substrate; the conductive layer is comprised of copper; the dielectric layer is comprised SiOCH; the anti-reflective coating layer is comprised of SiON; the etch stop/liner layer is comprised of Si₃N₄, SiOCN, SiOC or SiC; and the protective film portion is comprised of C₂H₄ or C₂H₆.

46. (Original) The method of claim 43, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of less than about 3.0.

47. (Original) The method of claim 43, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.0 to less than about 3.0.

48. (Original) The method of claim 43, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.5 to 2.8.

49. (Original) The method of claim 43, wherein the conductive layer has a thickness of from about 3000 to 15,000Å; the dielectric layer has a thickness of from about 2000 to 20,000Å; the anti-reflective coating layer has a thickness of from about 50 to 2000Å; the etch stop/liner liner has a thickness of from about 50 to 2000Å; and the protective film portion has a thickness of from about 50 to 2000Å.

50. (Original) The method of claim 43, wherein the conductive layer has a thickness of from about 3000 to 8000Å; the dielectric layer has a thickness of from about 2000 to 15,000Å; the anti-reflective coating layer has a thickness of from about 100 to 1500Å; the etch stop/liner liner has a thickness of from about 100 to 1000Å; and the protective film portion has a thickness of from about 200 to 1500Å.